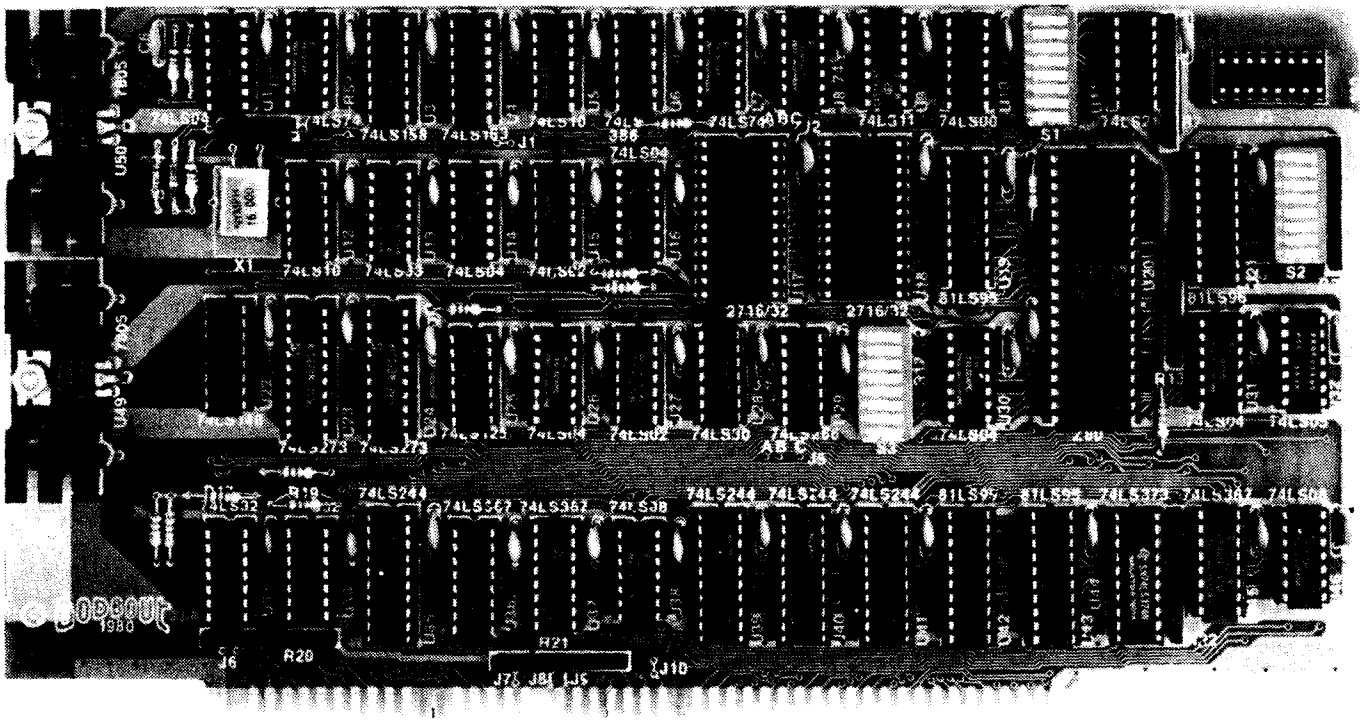
CPU-Z
USER'S MANUAL



IEEE S-100

4·6 MHz CPU

with onboard RAM/ROM & interrupt control

160 mac

CompuPro™ from GODBOUT

10/80

ABOUT CPU-Z

Congratulations on your decision to purchase the **CPU Z** board, specifically designed for electrical and mechanical compatibility with the IEEE S-100 bus standard. The S-100 bus is the professional level choice for commercial, industrial, and scientific applications. This bus provides for ready expansion and modification as the state of the computing art improves. We believe this board, along with the rest of the S-100 portion of the **CompuPro** family, is one of the best boards available for that bus.

As amateur radio operators have contributed greatly to communication technology, so too the computer hobbyist has provided the microcomputer industry with many significant developments. In recognition of this fact, we also make this board available in **"UNKIT"** form for those who enjoy the challenge of assembling and testing a fine computer board.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing a **CompuPro CPU Z** board...welcome to the club!

TECHNICAL OVERVIEW

The **CPU Z** was specifically designed to give the user one of the best Z80 CPU boards for the S-100 bus. The board features on-board PROM sockets, a power-on-jump circuit to any 256 byte boundary, a Memory Manager to extend the addressing range of the system from 64K-bytes to a maximum of 16M-bytes of system RAM, fully maskable vectored interrupts to speed up system throughput by eliminating polling loops, and wait state generation circuitry for all machine cycles.

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky TTL and MOS technology integrated circuits for reliable, cool operation. All this and sockets for all IC's go into a double sided, solder masked printed circuit board with a complete component legend.

USING THE VECTORED INTERRUPTS

The CPU chip recognizes 8 instructions as Restart0 - Restart7. These instructions will cause the program counter to jump to one of eight locations depending on the Restart instruction.

RESTART	Program Counter(HEX)
0	0
1	8
2	10
3	18
4	20
5	28
6	30
7	38

At these locations, jumps to interrupt driver routines can be placed into either RAM or PROM. Then when one of the VI0 - VI7 lines goes low, the specific routine can instantly be started to service the interrupting device. Upon Power-on-Clear or reset (RESET*) the interrupt mask is cleared, enabling all eight interrupt lines (NOTE: This does NOT mean that the Z80 has interrupts enabled.). Then (with the VI switch (SW3-8) turned ON) when any of the VI inputs goes low the Restart will be generated if the CPU has previously received an Enable Interrupts (FB(H)) command. To disable an individual interrupt line, or a group of lines, the mask must be set up by an output to Port FE(H) with the desired mask in the Accumulator. A "1" in the mask will disable the interrupt line, and a "0" will enable the interrupt line.

If it is desired to use this **CPU Z** board with the Z80 mode 2 interrupts, the on-board vector generation circuitry must be disabled. To do this switch SW3-8 should be turned OFF, and all 1's should be output to the interrupt mask port (Port FE(H)). This will prevent the **CPU Z** from responding to the V.I. lines, but it will still respond to the bus interrupt signal (bus pin 73).

EXAMPLE	(HEX)	(BINARY)
to disable VI5-VI7	07	(00000111)
to disable VI2	20	(00100000)
to disable all	FF	(11111111)

Note that the VI lines are all open collector and more than one device can be connected to each VI line by using open collector gates.

It is recommended to put a "DEAD MEMORY" error recovery routine at location 38 (H), since this location will be jumped to in case the CPU encounters an FF (H) instruction, which corresponds to a restart 7. This is the instruction that will be read from a memory location for which there is no system memory. Location 38 is the most common launching pad for CPU flights into never-never land.

USING THE NONMASKABLE INTERRUPT

The S-100 BUS has a NMI* pin (bus pin 12) which is implemented on the CPU card for any function that the user desires. NMI* is primarily used for a catastrophic system failure, such as loss of primary power. This interrupt enables the processor to execute a short program to save current system parameters on either a disc or some other nonvolatile memory before total power is lost (which usually takes milliseconds, lots of time for a computer). The NMI* causes the CPU to jump to address 66(H), which should be initialized with a routine to control the interrupt.

EXTENDED ADDRESSING

Address lines A16-A23 are driven through output port FD(H) and can be changed with a simple output instruction. Upon Power-on-Clear or reset (RESET*) the extended address lines will be reset to 0, bringing the system up in base page. To access memory in other than base page requires an output to Port FD(H) with the desired page address in the Accumulator in order to set the extended address lines A16-A23. These address lines are pin numbers 16, 17,15, 59, 61, 62, 63, & 64, for address lines A16-A23 respectively.

Example shown below:

ACCUMULATOR DATA TO ACCESS PAGE		
(HEX)	(BINARY)	(HEX)
40	01000000	40
2	00000010	2
F0	11110000	F0

Of course, to take advantage of this extended addressing feature requires memory boards which respond to extended address lines. If a board does not monitor the S-100 extended address lines, then only the normal 16 address lines will be decoded.

WAIT STATES

A single wait state may be added to any processor cycle by closing the corresponding dip switch on SW1. A wait may be added to:

CYCLE	SWITCH POSITION
PROM	1
I/O	2
MEMORY	3
INSTRUCTION	4

Due to critical timing requirements of the Z80 during an instruction fetch (M1), extra time may be required for marginally slow memory chips. When running at 4 MHZ some RAM chips may also need more time for each memory operation than is normally allowed. The on board PROM sockets may be used for many different speed PROM's, and when running at 4 MHZ a wait state may be needed for a fetch there also. The I/O wait should rarely be needed because of the fact that few I/O boards run slow and the Z80 automatically generates one I/O wait state, but the provision is made to the user.

ON-BOARD-MEMORY SOCKETS

The MEMORY sockets on this board are set up to take INTEL 2716, T.I. 2516 2Kx8 EPROMS, or any of the new 2Kx8 RAM chips which are pin compatible (Hitachi HM6116 or equivalent). By cutting J2(A-B) on the solder side above U17, J4 on the solder side to the left of U29, an J5(A-C) on the solder side beside U29 and installing jumpers J2(A-C) and J5(A-B) the sockets can now be used for 2732 4Kx8 EPROMS. (NOTE: Extreme care must be used when soldering in the jumpers so as not to damage the board or any of the traces. A soldering iron of no more than 25 watts should be used.) With 2732's SW3-4 is no longer used to address the sockets. The on-board sockets will be totally disabled when switch SW3-5 is ON. With SW3-6 ON, the sockets are addressable anywhere in base page (A16-A23 are all 0) on a 4K boundry (8K for the 2732's). This feature allows the user to have MEMORY in base page only. With SW3-6 OFF, the sockets ignores address lines A16 - A23 and occupies every page of memory. A prime example of how to use the sockets in this "shadow" mode would be to use them with SW3-6 turned ON and the Power-on-jump set to the start of the PROM address, then when the system is initially turned on the program in the PROM will start and either initialize the system by booting in a disk program, or some other type of routine. Then the last thing the PROM will do is jump to the RAM address where the initialization routine was loaded. The first thing that program will do is an output to port FD(H) of anything except 0. This will set the extended page address to the page that was in the Accumulator, and the sockets will be disabled. RAM which was overlapped with the PROM can now be used and a complete memory map is available to the user. SW3 positions 1-4 are used for address lines A15-A12. The socket closest to the Z80 chip is the low address half PROM and the right socket the high half.

Example:

SWITCH S3				DESIRED START ADDRESS (HEX)	
1	2	3	4	2716	2732
0	0	0	0	0000-0FFF	0000-1FFF
0	0	0	1	1000-1FFF	
0	0	1	0	2000-2FFF	2000-3FFF
0	0	1	1	3000-3FFF	
:	:	:	:	: :	: :
:	:	:	:	: :	: :
1	0	1	0	A000-AFFF	A000-BFFF
:	:	:	:	: :	
1	1	1	1	F000-FFFF	
		ON = "0"		OFF = "1"	

To disable ROM completely, turn ON SW3-5

CLOCK

The clock for this system can be set to allow the CPU to run at either 2MHZ or 4MHZ. SW1-5 is used to select between these two speeds. When SW1-5 is ON the CPU will run at 2MHZ and bus pin 24 (ϕ) will have a 2MHZ square wave on it. When SW1-5 is OFF, the system will run at 4MHZ and bus pin 24 will have a 4MHZ square wave on it. With a 24MHZ crystal used for X1 the speed switch SW1-5 will select between processor speeds of 6MHZ (when ON) and 3MHZ (when OFF). Bus pin 49 (CLK) will always have a 2MHZ signal on it.

POWER-ON-JUMP/JUMP-ON-RESET

Provisions have been made on this board to allow the processor to jump to any memory location on a 256 byte boundary on either a power-on only, or every reset also. To enable this feature, JMP ENABLE (SW1-8) should be turned ON and the jump address should be set on switch S2 according to the table below. To enable the jump on every reset also, SW3-7 should also be turned ON.

SWITCH POSITION	FUNCTION		
1	"	A15	
2	"	A14	
3	"	A13	
4	"	A12	ON = "1"
5	"	A11	OFF = "0"
6	"	A10	
7	"	A9	
8	"	A8	

EXAMPLE: To jump to E900 for a North Star floppy disc system, S2 positions 1-3,5, and 8 should be ON and S2 positions 4,6,and 7 should be OFF. JMP ENABLE (SW1-8) should be ON to enable this feature.

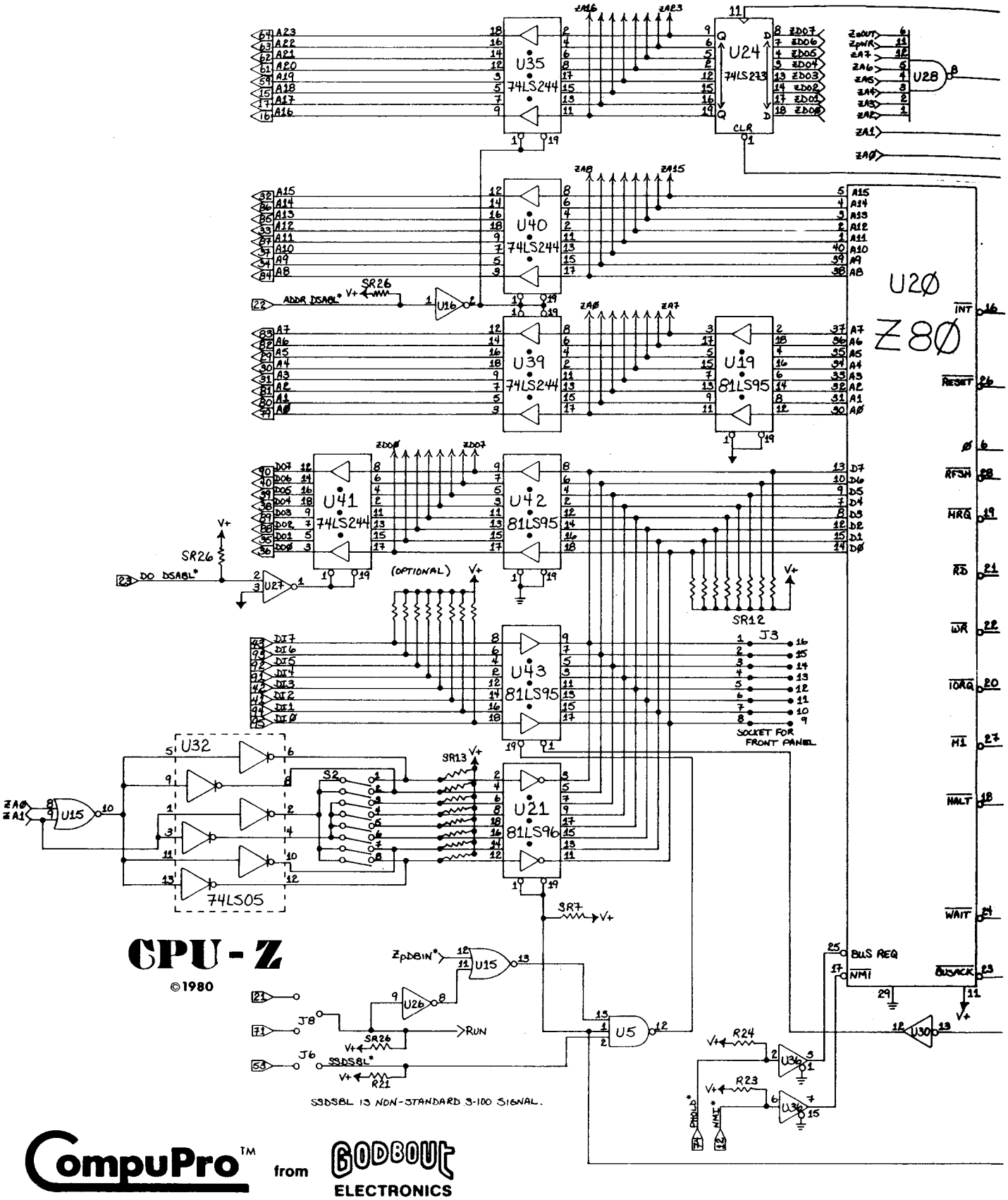
NOTE: Since the jump circuitry disables the input buffer, it is unnecessary to use the phantom line (S-100 pin 67) for proper operation.

MWRITE GENERATION

The CPU Z has circuitry on board for generating the MWRITE signal (bus pin 68) and a positive going strobe will be generated for each memory write operation. This circuitry looks at the bus and whenever the sOUT signal is low, and the pWR* signal strobes low, a MWRITE strobe will be generated. This signal must be generated at only one source in each system. If there is a front panel in your system it also may be generating the MWRITE signal, and the signal from the CPU Z must be disabled. There are two ways to disable this signal: A) Cut jumper J7 on the solder side below U36 and R26; or B) Remove pin 9 of U36 from its socket and let the pin hang out, this makes it easier to reconnect the pin should you ever want MWRITE to be generated from the CPU Z board in the future. If MWRITE is generated in more than one place, memory boards that rely on MWRITE as their write strobe may not work properly.

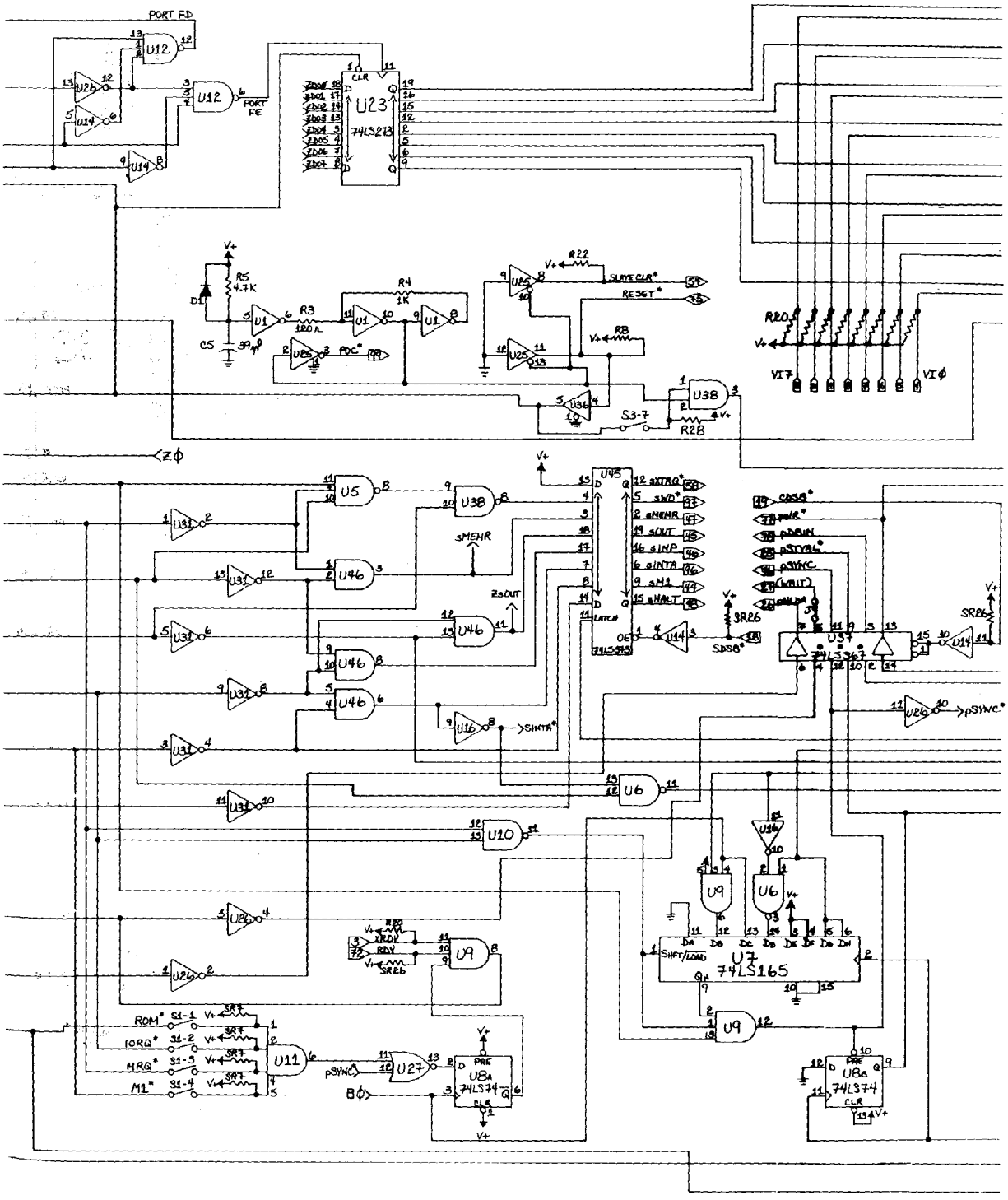
IMSAI FRONT PANEL USAGE

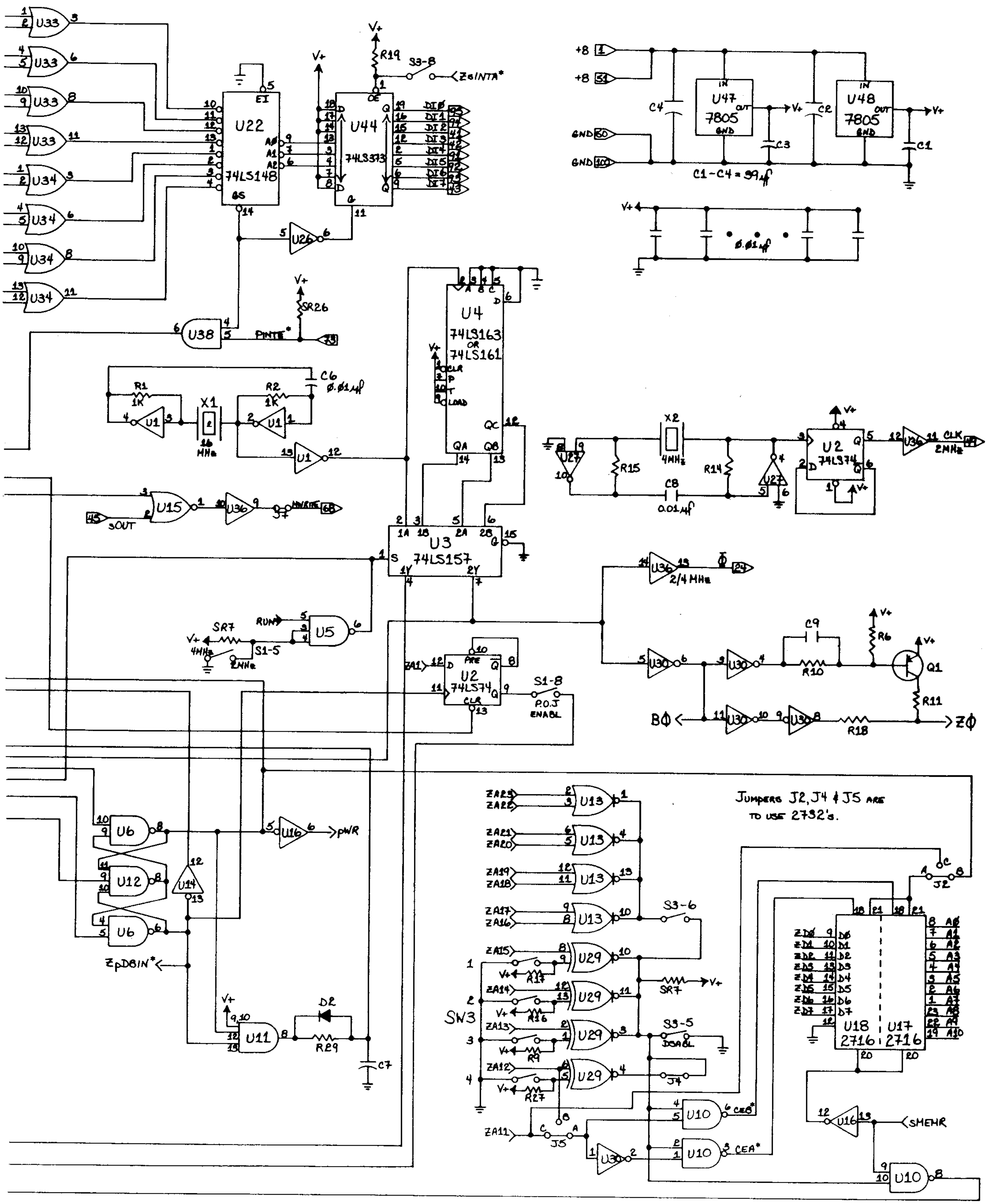
Although we will soon be manufacturing a front panel that will be fully compatible with the IEEE standard, if you have an IMSAI type front panel this CPU will require minor modifications to work properly. The problems arise from the fact that the IMSAI front panel (which does not conform to the IEEE standard) requires some signals that are not on the S-100 bus. Jumper pads are provided to allow these lines to be used. J6, and J8 should be installed to connect bus pins 53, and 71 respectively to control the CPU from the front panel. When the system is set to run at 4MHZ, the front panel will force the CPU to run at 2MHZ when the RUN/STOP signal is in the STOP mode. This will allow for proper front panel operation which is speed dependent. Socket J3 in the upper right corner is for the front panel connector. The CPU MWRITE circuitry will also have to be disabled if the front panel is going to generate MWRITE (bus pin 68). Jumper J9 can be installed to have the CPU drive bus pin 27 (which was the WAIT line), but this is not necessary for proper system operation.



CPU-Z

CompuPro™ from GODBOUT ELECTRONICS


PORT FD
PORT FE
U12
U26
U14
U23
74LS273
CLR
R5
4.7K
R3
180Ω
R4
1K
C5
39μ
PDC*
R22
SLAVE CLR*
RESET*
R8
R20
VI7
VIØ
U38
S3-7
R28
ZØ
U5
U38
sMEMR
U46
ZsOUT
U45
74LS373
sXTRQ*
sWD*
sMEMR
sOUT
sINP
sINTA
sM1
sHALT
LATCH
OE
SR26
SDSØ*
U34
74LS367
CASØ*
pWR*
pRDIN
pSTVAL*
pSYNC*
pSYNC*
sINTA*
U6
U10
U26
U9
U6
U7
74LS165
SHIFT/LOAD
RDY
SR25
ROM*
IORQ*
MRQ*
M1*
S1-1
S1-2
S1-3
S1-4
SR3
SR4
SR5
SR7
U11
U27
pSYNC
BØ
U8a
74LS74
PRE
CLR
U8b
74LS74



U33
U34
U22
74LS148
U44
74LS373
R19
S3-8
ZSINTA*
+8
GND
U47
7805
U48
7805
C1-C4 = 39µf
Ø.Ø1µf
U38
PINTE*
SR26
U4
74LS163
OR
74LS161
R1
1K
R2
1K
X1
16 MHz
C6
Ø.Ø1µf
X2
4MHz
R15
R14
C8
0.01µf
U27
U2
74LS74
U36
CLK
2MHz
U15
SOUT
J7
MWRITE
U3
74LS157
Φ
2/4 MHz
RUN
U5
SR7
4MHz
2MHz
S1-5
S1-8
P.O.J
ENABL
C9
R6
R10
Q1
R11
R18
BΦ
ZΦ
U6
U12
U14
U16
pWR
ZpDBIN*
U11
D2
R29
C7
U13
Jumpers J2, J4 & J5 are to use 2732's.
S3-6
U29
SR7
SW3
R17
R16
R9
R27
S3-5
DSABL
J4
J5
J2
U10
CEB*
CEA*
U18
2716
U17
2716
SMEMR

VECTORED INTERRUPTS AND MASK

Upon reset (RESET*) U23 is cleared, and will output all lows to the Or-gates (U33 & U34). The VI0 - VI7 inputs normally sit at a high level, and hence all inputs on U22 are high. This resting state makes the GS output high. Upon receiving a vectored interrupt when one of the VI0 - VI7 inputs goes low, U22 will output a value corresponding to the highest priority interrupt on the lines. This value will go to U44 and when the CPU acknowledges the interrupt, the proper Restart command will go to the CPU. When a 1 has been written into the mask port FE(H), U23 will output a high to the associated Or-gate (U33 & U34). Then when an interrupt pulls the input low, U22 will still have a high input and will never detect interrupts that are being masked out.

EXTENDED ADDRESSING

When an OUT FD(H) instruction is executed, the data bits in the Accumulator are latched into U24 and output on bus lines A16-A23. These address lines will be tri-stated along with the other 16 address lines when ADDR-DSABL (Bus pin 22) is driven low by an external device requesting control of the bus.

CPU STATUS LINES

The S-100 bus has eight status signals that all bus masters must provide, these signals come from U45. During either a read cycle or a write cycle these status signals are latched on the bus. A short time after the read or write signal goes away the status signals are allowed to toggle. The S-100 status signals are shown below, along with their associated bus pins. (A * suffix means active low signal.)

SIGNAL	BUS PIN
sWO*	97
sMEMR	47
sINTA	96
sM1	44
sINP	46
sOUT	45
sHLTA	48
sXTRQ*	58

These status bits are decoded from the seven control signals coming from the Z80 as shown below:

STATUS SIGNALS

CONTROL SIGNAL	sWO* (a) or (b)		sMEMR	sINTA	sM1	sINP	sOUT	sHLTA
RFSH*	1	X	X	X	X	X	X	X
MRQ*	0	X	0	X	X	X	X	X
RD*	1	X	0	X	X	0	X	X
WR*	X	0	X	X	X	X	0	X
IORQ*	X	X	X	0	X	0	0	X
M1*	X	X	X	0	0	X	X	X
HALT*	X	X	X	X	X	X	X	0

(A* suffix means active low signal)
An X means a don't care condition.
The SXTRQ* signal is permanently high since this is an 8 bit processor.

SYSTEM CLOCK

The system clock circuitry consists mainly of U1, U3, and U4. The 16 MHZ square wave is fed into U4 which divides it down to the desired system clock speed. The multiplexer U3 will feed either 16 MHZ or 8 MHZ to the pSYNC and pSTVAL* generation circuitry and 2MHZ or 4MHZ to the Z80 and bus for the system clock. The Z80 clock has inverters from U30 along with some discrete devices for providing the required clock rise and fall time. If jumper J8 is used, then when the RUN LINE (bus pin 71) is low the input to U5 will be low and cause the system to run at 2 MHZ. This is the same circuitry that switch SW1-5 uses to determine the system speed. The 2MHZ clock for bus pin 49 is generated with crystal X2, inverters in U27, and a flip-flop in U2 which is then fed through a buffer to bus pin 49.

POWER-ON-JUMP(POJ)/JUMP-ON-RESET(JOR)

The jump circuitry consists of octal inverter U21 (81LS96), DIP switch SW2, SIP resistor R23, hex o.c. inverter U32 (74LS05), a "D" flip flop U2, the POJ enable switch SW1-8, and JOR enable switch SW3-7. With the POJ enable switch ON, upon receiving a power-on-clear, the "D" flip flop is cleared which disables input buffer U43, and enables jump buffer U21. This action starts a three byte sequence which will cause the CPU to jump to the proper starting location. The CPU is reset to address 0, and from the jump buffer a jump (C3H) instruction is put on the data bus. At address 1 the low order address of zero is then put on the data bus, then at address 2 the high order address coming from the jump switch setting is placed on the data bus. When address 2 is in the address buffer the "D" flip flop will then be clocked to the set state and disable the jump buffer while enabling the data input buffer. The "D" flip flop will not get cleared again until the next POC. This complete sequence also occurs for every RESET*, if switch SW3-7 is turned ON. This option will allow the CPU to come up with a known jump on power-on and then later when a reset is recognized the CPU can either start again at 0(H) or jump to the address in switch SW2.

WAIT STATES

The CPU wait line (Z80 pin 24) is driven by three main sources, causing the processor to give more time for certain devices or system states. The three sources are; a) The RDY (pin 72) bus signal, which will be driven by an external device which must have more time to respond to the CPU, b) The XRDY (pin 3) bus signal which is driven by the front panel (if the system has one), and c) On board selector to generate a wait state for four different states. The on-board wait state will come from the settings of SW1 positions 1-4. M1 (SW1-4) will generate a wait state for every instruction cycle. The MRQ (SW1-3) will generate a wait state for every memory fetch cycle. The IORQ (SW1-2) will generate a wait state during every I/O operation. Finally, the ROM switch (SW1-1) will generate a wait state for every access of the on-board MEMORY. U8 will remain in the clear mode with Q* high unless one of these switches (SW1 positions 1-4) is turned ON. Then when one of the selected inputs go low, U8 will be set and cause the wait input (on the CPU) to go low. These wait states can only start when pSYNC is high. When pSYNC goes low U8 will be clocked low with the next negative edge of the system clock.

SWITCH SUMMARY

S1 POSITION	FUNCTION
1	WAIT STATE FOR ROM
2	WAIT STATE FOR I/O
3	WAIT STATE FOR MEMORY FETCH
4	WAIT STATE FOR INSTRUCTION FETCH
5	SPEED SWITCH (OFF = 4 MHZ.)
6	NOT USED
7	NOT USED
8	POWER-ON-JUMP ENABLE

S2 POSITION	FUNCTION	
1	JUMP ADDRESS BIT A15	
2	JUMP ADDRESS BIT A14	
3	JUMP ADDRESS BIT A13	ON = "1"
4	JUMP ADDRESS BIT A12	OFF = "0"
5	JUMP ADDRESS BIT A11	
6	JUMP ADDRESS BIT A10	
7	JUMP ADDRESS BIT A9	
8	JUMP ADDRESS BIT A8	

S3 POSITION	FUNCTION	
1	SOCKET ADDRESS BIT A15	ON = "0" OFF = "1"
2	SOCKET ADDRESS BIT A14	
3	SOCKET ADDRESS BIT A13	
4	SOCKET ADDRESS BIT A12	
5	SOCKET DISABLE (WHEN ON)	
6	SOCKET BASE PAGE ONLY (WHEN ON)	
7	JUMP-ON-RESET ENABLE	
8	INTERRUPT ENABLE FOR VECTORED INTERRUPTS	

JUMPER SUMMARY

J2 - Used with J4, J5, to convert memory sockets for 2732 use

J3 - Front panel data socket

J4 - See J2

J5 - See J2

J6 - SSDSBL for IMSAI type systems

J7 - MWRITE brought to Bus pin 68

J8 - Run or single step for IMSAI type systems

J9 - WAIT brought to Bus pin 27

Parts List

(1) **CPU Z** circuit board

INTERGRATED CIRCUITS (NOTE: the following parts may have letters, suffixes and prefixes along with the key numbers given below.)

(2)	74LS00	quad 2 input NAND	(U6, U10)
(2)	74LS02	quad 2 input NOR	(U15, U27)
(6)	74LS04	hex inverter	(U1, U14, U16, U26, U30, U31)
(1)	74LS05	hex inverter o.c.	(U32)
(2)	74LS08	quad 2 input AND	(U38, U46)
(2)	74LS10	triple 3 input NAND	(U5, U12)
(1)	74LS11	triple 3 input AND	(U9)
(1)	74LS21	dual 4 input AND	(U11)
(1)	74LS30	8 input NAND	(U28)
(2)	74LS32	quad 2 input OR	(U33, U34)
(1)	74LS33	quad 2 input NOR o.c.	(U13)
(2)	74LS74	dual "D" flip flop	(U2, U8)
(1)	74LS125	quad buffers	(U25)
(1)	74LS148	octal encoder	(U22)
(1)	74LS158	quad 2-to-1 mux.	(U3)
(1)	74LS161/3	4 bit counter	(U4)
(1)	74LS165	8 bit shift register	(U7)
(4)	74LS244	octal bus driver	(U35, U39-41)
(1)	74LS266	quad 2 input XNOR	(U29)
(2)	74LS273	octal latches	(U23, U24)
(2)	74LS367	hex bus driver	(U36, U37)
(2)	74LS373	octal latches	(U44, U45)
(3)	81LS95	octal bus driver	(U19, U42, U43)
(1)	81LS96/98	octal bus inverter	(U21)
(1)	Z80A	Z80 microprocessor	(U20)
(2)	7805	5 volt regulator	(U47, U48)
(1)	2N3906	PNP transistor	(Q1)

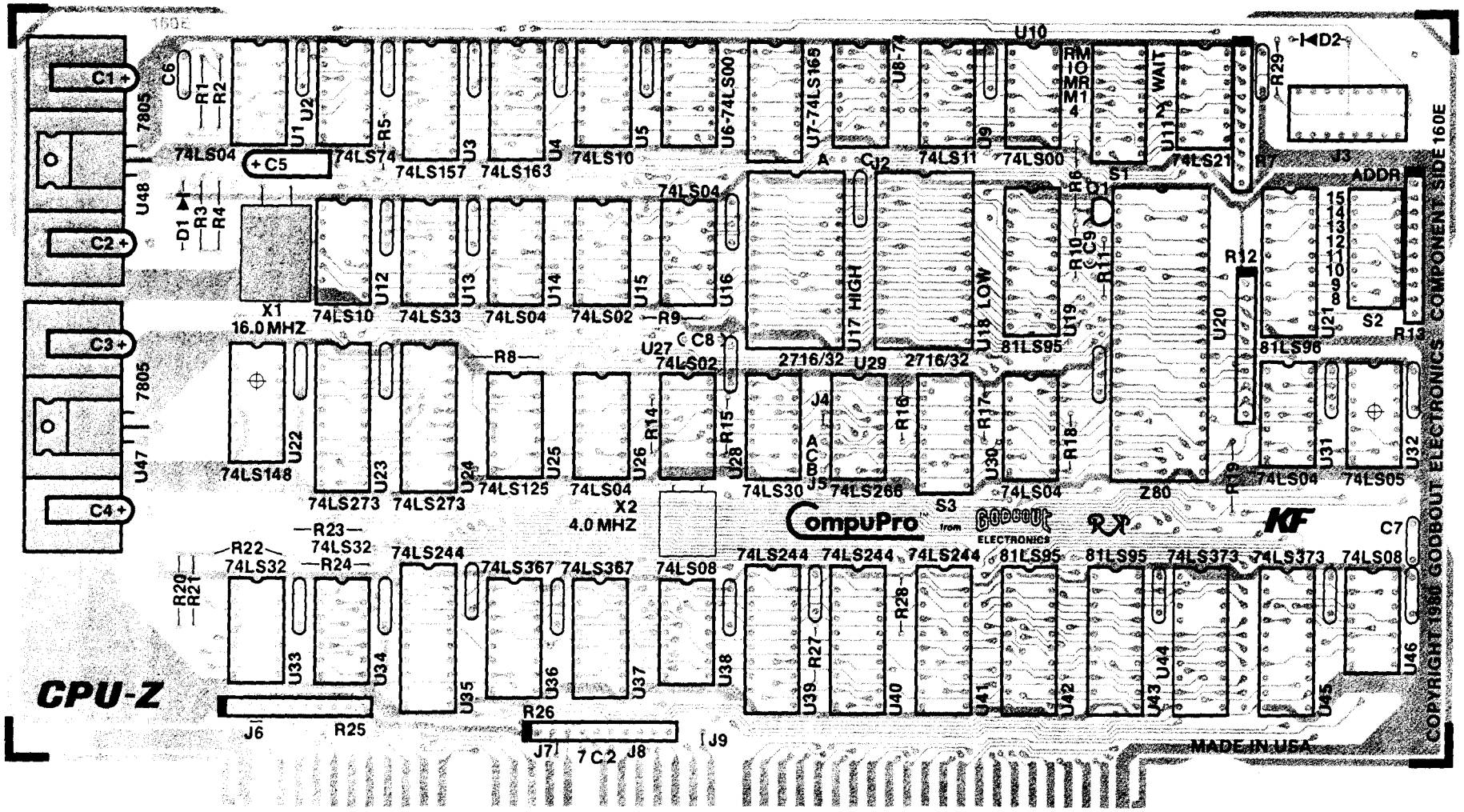
OTHER ELECTRONIC COMPONENTS

(5)	SIP resistor packs	(SR7, SR12, SR13, SR25, SR26)*
(5)	39uf Tantalum capacitors	(C1 - C5)
(1)	390 - 430 pF capacitor	(C7)*
(1)	43pf capacitor	(C9)*
(27)	Ceramic Bypass capacitors	All OTHER*
(2)	33 ohm resistors c.f.	(R11, R18)*
(1)	120 ohm resistor c.f.	(R3)*
(1)	150 ohm resistor c.f.	(R6)*
(1)	390 ohm resistor c.f.	(R29)*
(1)	910 ohm resistor c.f.	(R10)*
(5)	1K ohm resistors c.f.	(R1, R2, R4, R14, R15)*
(6)	1.5K ohm resistors c.f	(R8, R20 - R24)*
(7)	4.7K ohm resistors c.f	(R5, R9, R16, R17, R19, R27, R28)*
(1)	16MHz crystal	(X1)
(1)	4MHz crystal	(X2)
(2)	Glass signal diodes	(D1, D2)*

MECHANICAL COMPONENTS

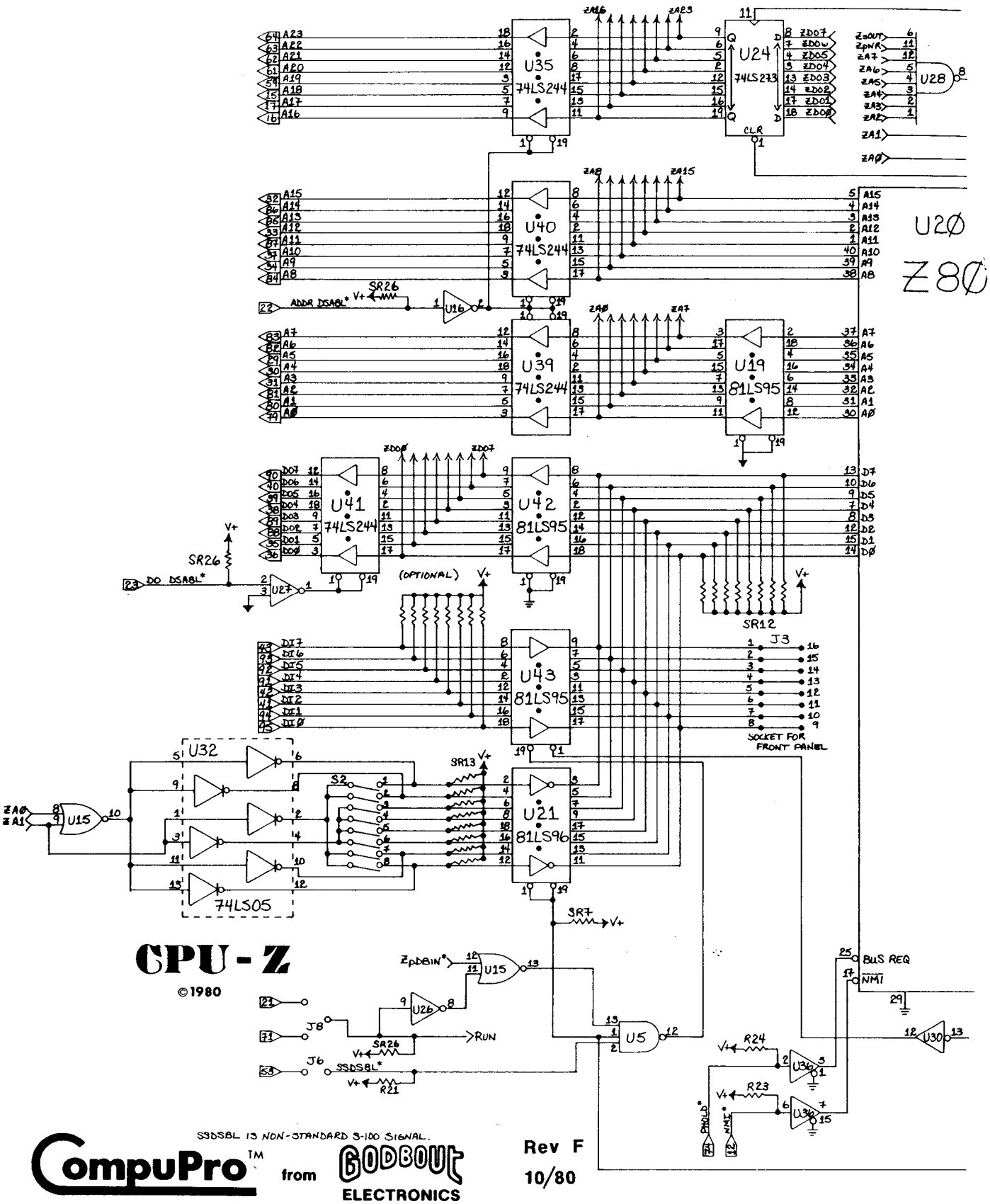
(46)	Low profile sockets*	
(3)	Dip switch, 8 position	(S1-S3)*
(2)	TO-220 heat sinks	
(2)	Sets 6-32 hardware	
(2)	Card extractors	

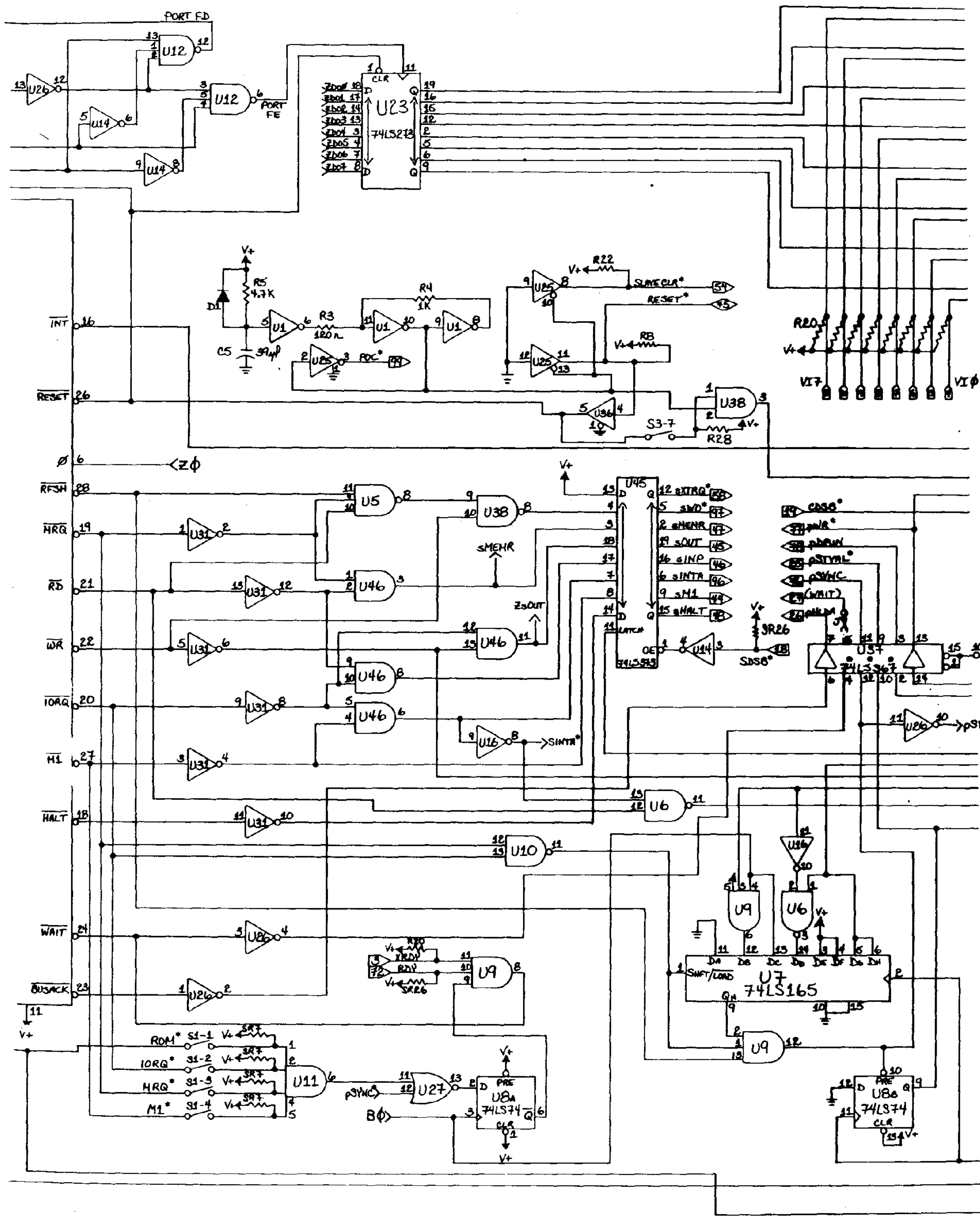
* supplied already soldered on the board

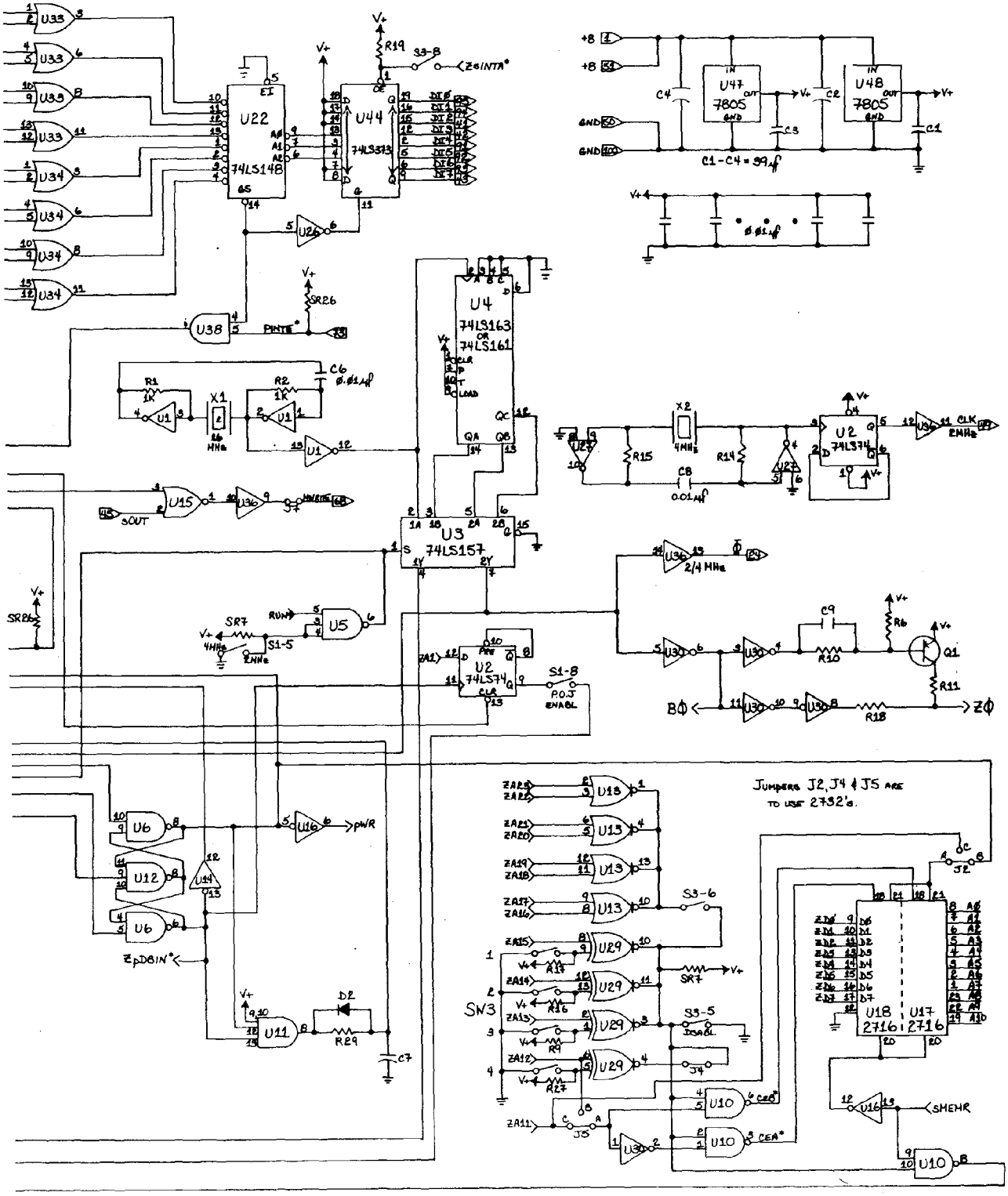


Component Layout

UP


U20
Z80
U35
74LS244
U24
74LS273
U28
U40
74LS244
SR26
ADDR DSABL*
U16
U39
74LS244
U19
81LS95
U41
74LS244
U42
81LS95
(OPTIONAL)
SR26
DO DSABL*
U27
SR12
J3
U43
81LS95
SOCKET FOR FRONT PANEL
U32
74LS05
U15
S2
SR13
U21
81LS96
SR7
CPU - Z
©1980
ZpDBIN*
U15
U26
J8
RUN
SR26
J6
SSDSBL*
R21
U5
BUS REQ
NMI
U30
R24
U36
R23
U36
PHOLD*
NMI*
SSDSBL IS NON-STANDARD S-100 SIGNAL.
CompuPro™ from GODBOUT ELECTRONICS
Rev F
10/80


PORT FD
PORT FE
U12
U14
U26
U23
74LS273
CLR
INT
RESET
RFSH
MRQ
RD
WR
IORQ
M1
HALT
WAIT
BUSACK
V+
R5
4.7K
D1
C5
R3
R4
1K
U1
U25
POC*
R22
SLAVE CLR*
RESET*
R8
U36
U38
S3-7
R28
VI7
VIφ
R20
<Zφ
U5
U31
U46
U45
74LS373
sMEMR
ZsOUT
LATCH
OE
sINTA
sM1
sHALT
sOUT
sINP
SINTA*
U16
U14
SDSB*
CDSB*
pDBIN
pSTVAL*
pSYNC
pHLDA
SR26
U37
74LS367
U86
pSYNC*
U6
U10
U9
U7
74LS165
SHFT/LOAD
XRDY
RDY
ROM*
IORQ*
MRQ*
M1*
S1-1
S1-2
S1-3
S1-4
SR7
U11
U27
U8A
74LS74
Bφ
PRE
U8B


U22
74LS148
U44
74LS373
R19
S3-8
Z6INTA*
U33
U34
U38
PINTE*
SR26
U4
74LS163
OR
74LS161
U3
74LS157
U2
74LS374
U47
7805
U48
7805
C1-C4 = .99μf
.01μf
X1
4MHz
R1
1K
R2
1K
C6
.01μf
U15
SOUT
U36
SR7
RUN
S1-5
ENHz
S1-8
POJ
ENABL
2/4 MHz
C9
R10
R6
Q1
R11
R18
BΦ
ZΦ
U6
U12
U14
U16
PWR
ZpDBIN*
U11
D2
R29
C7
U5
U18
U13
U29
U10
S3-6
S3-5
SR7
SW3
R16
R17
R27
J4
J5
J2
JUMPERS J2, J4 & J5 ARE
TO USE 2732's.
U18
2716
U17
2716
SMEMR